## REMARKS/ARGUMENTS

Claims 6-25 are pending. Claims 6 and 14 have been amended. No claim has been added or canceled. No new matter has been added.

Claims 6-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsu in view of Gill and Stewart. Applicants respectfully traverse the rejection.

Claim 6 relates to a source side programming device. Conventional single gate/transistor flash memory devices perform programming operations by charging the floating gate with injection of hot channel electrons from the drain side. In the claimed embodiment, the flash memory has transistors that have, respectively, a single control gate and a single floating gate for source side programming.

Hsu is directed to a self-aligned buried channel stacked gate flash memory cell. Hsu discloses a single-transistor-cell device, where no more than one transistor is required to program a cell. Hsu programs the flash memory cell by applying a voltage to the drain, as is the conventional technique. Hsu does not provide any motivation or suggestion for modifying this programming operation to source side programming. That is, Hsu does not appreciate the benefits of the source side programming, unlike the present inventors (see page 6). Accordingly, Hsu does not teach a person skilled in the art a flash memory device that is configured for source side programming.

Gill is directed to a memory cell array for a non-volatile memory device having single-transistor cells that are arranged in a matrix of rows and columns. As with Hsu, Gill applies a voltage to the drain to program a cell and does not provide any motivation or suggestion for performing source side programming.

Stewart is directed to a non-volatile memory having multiple transistors for a single cell (see Fig. 4). To program a bit, at least two transistors Pw and Ps are used. The device configuration disclosed in Stewart is incompatible with those of Hsu and Gill.

Although Steward discloses applying a voltage to a source region of the transistor Ps to program, this is done after the transistor Pw is turned on. Hsu and Gill does not have such a transistor Pw. A person skilled in the art, therefore, would not think of adopting the feature of

source side programming to the devices of Hsu and Gill based solely based on Stewart. The Examiner, however, argues that these three references may be combined since these all relate to the memory device and are "from the same field of endeavor."

Applicants disagree. Since Stewart discloses a device that has entirely different configuration as those of Hsu and Gill, a person skilled in the art would not normally think of combining these references without any specific motivation to combine them regardless of whether or not they are all in "the same field of endeavor." Even if they are combined for some reason, they would not be combined in the manner suggested by the Examiner since none of these references discloses the advantages of the source side programming. Such an advantage or need is only found in Applicant's specification. Therefore, without the benefit of hindsight obtained from the claimed embodiment, a person skilled in the art would not think of converting the devices of Hsu and Gill to source side programming devices.

It is well settled law that one cannot use hindsight to reconstruct the claimed invention by picking and choosing features from prior art. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification...It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."" *In re Fritch*, 23 USPQ 2d 1780, 1783-84, (Fed. Cir. 1992). Therefore, claim 6 is allowable.

Claim 14 recites, "...wherein the control gate is applied with a first voltage and the source region is applied with a second voltage to program the non-volatile device, wherein the floating gate, control gate, drain region, and source region together define a first transistor that is configured to store one bit of data, wherein the non-volatile device further includes a second transistor that is configured to store one bit of data, the second transistor including a source region that shares a common node with the source region of the first transistor." These features are not disclosed or suggested by the cited references. Claim 14 is allowable.

Claim 19 is also directed to a source side programming device. This feature is not disclosed or suggested by the cited references. Claim 19 is allowable at least for this reason. Other claims depend from one of the above independent claims and are allowable at least for this reason.

## CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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